

Fig. 1  
Prior Art

2/6

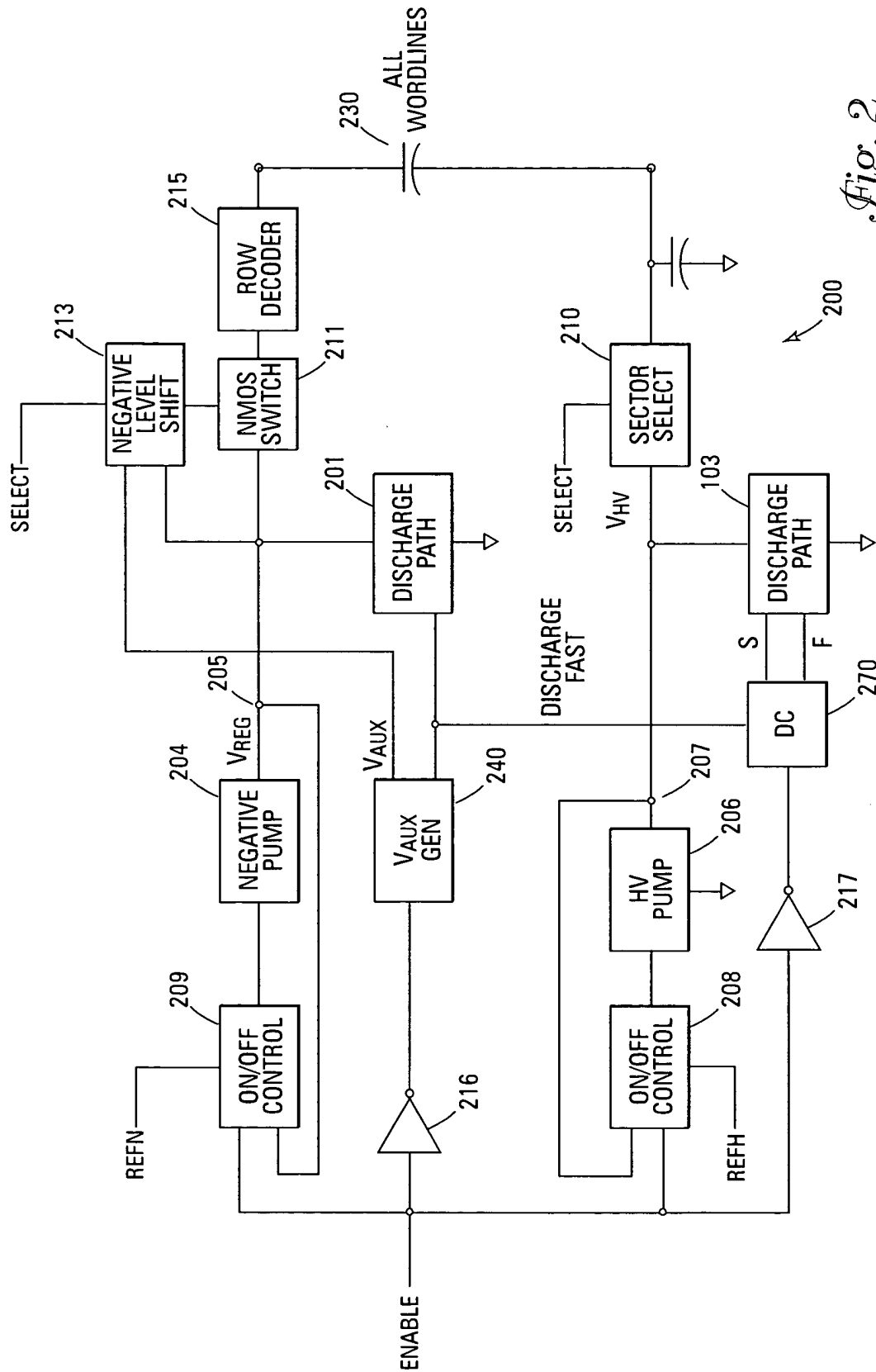


Fig. 2

3/6

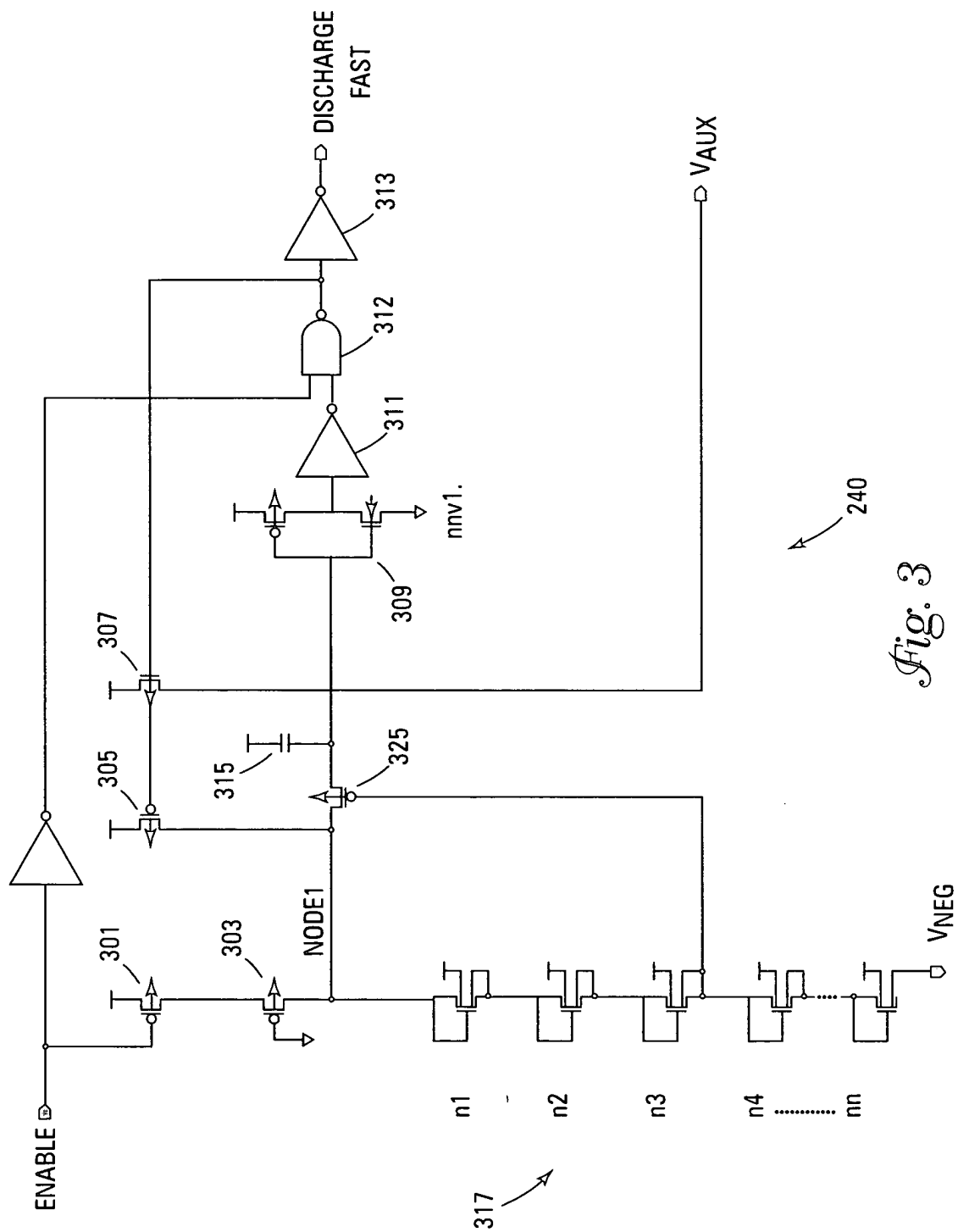
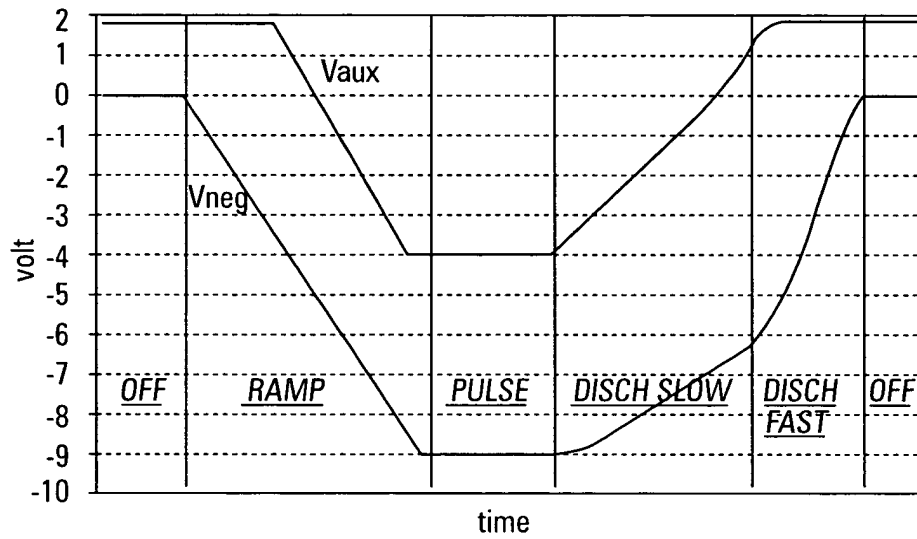


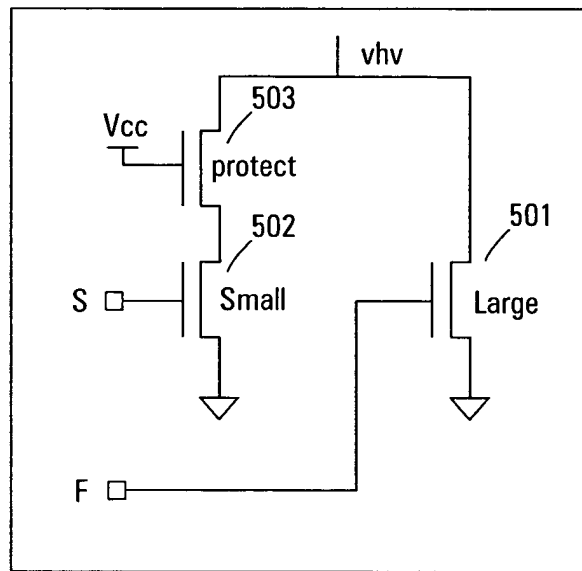
Fig. 3

4/6



*Fig. 4*

5/6



203

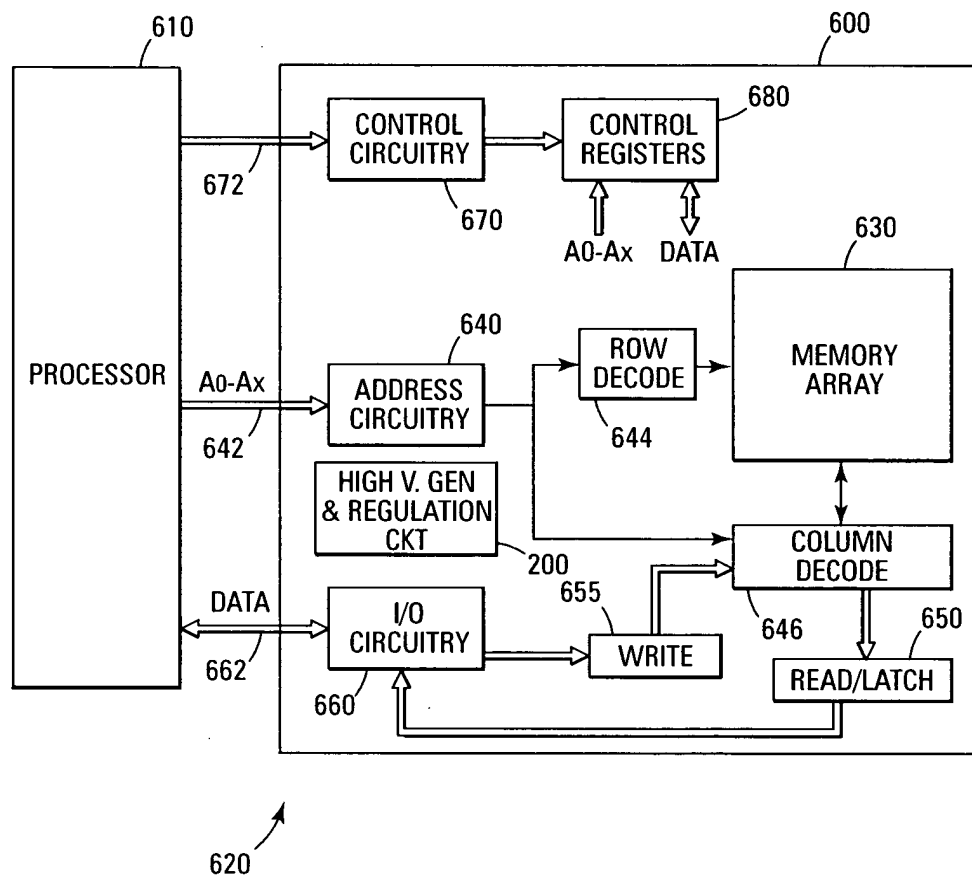
*Fig. 5*

DC block logic table.

enable	Disch fast	S	F
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	0

*Fig. 7*

6/6



*Fig. 6*